Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (previously presented) An IC comprising:

a memory cell array having a plurality of memory cells, wherein each memory cell includes at least a first port and at least a second port, the first and second ports of the memory cells forming at least first and second access ports of the memory cell array for accessing the memory cells;

a cache memory coupled to said first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory; and

a refresh control circuit for performing refresh operations for said memory cells.

2. (previously presented) An IC comprising:

a memory cell array having a plurality of memory cells, wherein the memory cell includes at least first and second ports forming a memory cell array with at least first and second access ports for accessing the memory cells;

a cache memory coupled to said first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said corresponding address and data portions contain valid address and data values; and

a refresh control circuit for performing refresh operations.

3. (previously presented) The IC according to claim 2, wherein said first and second access ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.

4. (previously presented) The IC according to claim 3, wherein said cache memory comprises an address comparator which is coupled to said address path of at least one of said first and second access ports.

5. (previously presented) The IC according to claim 4, wherein said address comparator compares an address being provided through at least one of said access ports and an address being provided from said address portion of said address memory, and in case of a match, outputs the data stored in the corresponding memory cell onto the data read path of said at least one of said access ports.

6. (previously presented) The IC according to claim 5, wherein in case of said match of addresses a refresh for a row of memory cells within the memory cell array is performed through the second access port.

7. (previously presented) The IC according to claim 6, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

8. (original) The IC according to claim 7, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and

second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

9. (previously presented) The IC according to claim 5, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

10. (original) The IC according to claim 9, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

11. (previously presented) The IC according to claim 1, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

12. (original) The IC according to claim 11, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

13. (previously presented) An IC comprising:

a memory cell array having a plurality of dynamic memory cells, wherein the memory cells comprise at least first and second ports to form a memory array having at least first and second access ports accessing the memory cells;

a refresh control circuit to perform a refresh for said memory cells once within a retention time interval;

a cache memory connected to at least one of said ports;

a switching device coupled to said at least one of said ports, said cache memory, and said memory cell array; and

said switching device being operated to connect either one of said memory cell array and said cache memory to said at least one of said access ports in response to a read operation.

14. (previously presented) The IC according to claim 13, wherein said refresh control circuit performs a refresh operation while a read operation is performed through at least one of said access ports from said cache memory.

15. (original) The IC according to claim 13, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said address and data portions contain valid address and data values.

16. (previously presented) The IC according to claim 13, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

17. (previously presented) An IC comprising:

a memory cell array having a plurality of memory cells with at least first and second ports forming a memory cell array with at least first and second access ports;

a cache memory coupled to said first and second access ports, wherein said cache memory can be accessed through either of said access ports;

said first and second access ports comprising address terminals and data terminals; and

said second access port being controlled by a refresh control circuit to perform a refresh of said memory cells.

18. (previously presented) An IC comprising:

a memory cell array having a plurality of memory cells with at least first and second ports forming a memory cell array with at least first and second access ports;

a cache memory coupled to said first and second access ports;

said first and second access ports comprising address terminals and data terminals; and

said second access port being controlled by a refresh control circuit to perform a refresh of said memory cells;

wherein a refresh operation is performed for a row of memory cells through said second access port, and a read command received through said second access port is performed through said cache memory in parallel to said refresh operation.

19. (previously presented) The IC according to claim 18, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

20. (previously presented) An IC comprising:

a memory cell array having a plurality of memory cells, wherein the memory cell includes at least first and second ports forming a memory cell array with at least first and second access ports, wherein at least one of the first and second ports are used for memory accesses; and

a cache memory coupled to at least one of the access ports used for memory accesses, wherein during a read operation to the memory cell array to obtain read data, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory; and

wherein the at least one of the first and second access ports used for memory accesses comprises an address path and a data read path, said address path connected to said address portion of said cache memory and said data read path of the at least one of the first and second access ports for memory accesses is connected to said data portion.

21. (cancelled)

22. (previously presented) The IC according to claim 20 comprises a refresh control circuit for performing refresh operations through the other of the first and second access ports.

23. (previously presented) The IC according to claim 20 wherein the at least first and second access ports are used for memory accesses.

24. (previously presented) The IC according to claim 23 wherein said first and second access ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.

25. (previously presented) The IC of claim 24 comprises a refresh control circuit for performing refresh operations through either one of the access ports.

26. (new) An IC comprising:

a memory cell array having a plurality of memory cells, wherein each memory cell includes at least a first port and at least a second port, the first and second ports of the memory cells forming at least first and second access ports of the memory cell array for accessing the memory cells;

a cache memory coupled to said first and second access ports;

a refresh control circuit for performing refresh operations for said memory cells;

wherein during a conflict between a read operation to the memory cell array and a refresh operation, the cache memory provides read data if the read data is contained therein or the read operation is stalled until the conflict is over if the read data is not contained in the cache memory.